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I. Main Educations (最高學歷):

Ph.D. of Electrical Engineering, National Tsing-Hua University

II. Research Fields (*Expertise* 研究專長):

- Power Electronics, BCD Process (HV, UHV)
- VLSI Reliability
- ESD/EOS Protection Design
- CMOS Latchup Free Design/Testing
- System EMC/EMS Testing and Troubleshooting

III. Relevant Certificates of Conformity (相關合格證照):

1. ESD S20.20 Induction and Practice 訓練合格

   (DNV.GL Certificate No.: 20.26.01P.011)

2. ESD S20.20: 2021 Induction Course 訓練合格

   (DNV.GL Certificate No.: 21.26.02P.007)

3. TAF 實驗室認證規範 ISO/IEC 17025 訓練合格

   (Certificate No.: TAF-QM110006-C-24)

4. TAF 測試實驗室主管訓練合格

   (Certificate No.: TAF-TH110008-C-05)

5. ESG 師資培訓與認證訓練合格

   (Certificate No.: TISDA-ESG-JM-20240063)

IV. Personal Experiences (履經歷):

- 台灣靜電放電防護工程學會 (理事) 2022/01 ~2024/12

- 應廣科技(股)公司 (顧問) 2021/09 ~2022/09
- 國立聯合大學 電資學院 院長 2021/08 ~
- 偉芯科技公司 (顧問) (2020/07) ~
- 台灣靜電放電防護工程學會 (理事) 2020/01 ~2021/12
- 台灣靜電放電防護工程學會 (理事) 2018/01 ~2019/12
- 十速科技(股)公司 (顧問) 2016/04 ~ 2016/12
- 國防科技發展研究中心 (審議委員) 2016/03 ~
- 國立聯合大學 材料與化學工程博士學位學程 (合聘教授) 2014/08 ~2017/07
- 深圳華為技術 (海思半導體)公司 (顧問) 2011/01 ~ 2012/03
- SunPalTech Co., LTD (顧問) 2010/05 ~
- 台灣靜電放電防護工程學會 (監事) 2010/01 ~ 2011/12
- ChipGoal Electronics Corp. (顧問) 2007/01 ~ 2009/09
- AU Optronics Corp. (顧問) 2005/10 ~ 2006/09
- 台灣靜電放電防護工程學會 (理事) 2003/07 ~ 2005/06
- 國立聯合大學 電子系 (系(所)主任) 2003/02 ~ 2005/07
- 閎康科技(股)公司 (首席顧問) 2000/08 ~ 2006/12
- Advances Electronic Technology Corp. (首席顧問) 2000/08 ~ 2005/12
- Prolific Technology Inc. (顧問) 2000/07 ~ 2002/06
- 工研院電子工業研究所 (顧問) 1998/09 ~ 2000/03

V. Personal Honors (個人榮譽事項)：

- 國立聯合大學 科技部補助大專校院研究獎勵 傑出研究連續三年(109-111)獎 (2023/11)
- 國立聯合大學 電資學院 傑出研究前 10 名獎 (2023/11)
- 國立聯合大學 電資學院 研究計畫績優類前 10 名獎 (2023/11)
- 2023 TSRI 優良晶片設計獎優等設計獎(指導教授) (2023/08)
- 111 年度科技部補助大專校院研究獎勵案 傑出研究獎 (2022/12)
- 國立聯合大學 電資學院 傑出研究前 10 名獎 (2022/11)
- 國立聯合大學 電資學院 研究計畫績優類前 10 名獎 (2022/11)
- 110 年度科技部補助大專校院研究獎勵案 傑出研究獎 (2021/11)
- 國立聯合大學 電資學院 傑出研究獎 (2021/11)
- 國立聯合大學 電資學院 研究計畫績優類前 15 名獎 (2021/11)

- 台灣學術新創學會(TAAI) 研究傑出表現獎 (2021/10)
- 110 年度聯合大學 傑出研究獎 (2021/08)
- 109 年度科技部補助大專校院研究獎勵案 傑出研究獎 (2020/11)
- 國立聯合大學 電資學院 傑出研究獎 (2019/12)
- 國立聯合大學 產學合作績優教師 優良獎 (2019/05)
- 107 年度科技部補助大專校院研究獎勵案 傑出研究獎 (2018/12)
- 國立聯合大學 電資學院 傑出研究獎 (2018/12)
- 107 年度聯合大學 傑出研究獎 (2018/08)
- 國立聯合大學 電資學院 傑出研究獎 (2017/12)
- 國立聯合大學 產學合作績優教師 優良獎 (2017/05)
- 2016 CIC 晶片製作優等設計獎(指導教授) (2016/08)

VI. Publication Papers & Projects (近年發表之論文與研究計劃):

A. Referred Journal papers: (2014~2023)

1. Xing Chen Mai, Shen-Li Chen*, Hung Wei Chen, Yi Mu Lee, "Impacts of Floating Poly on ESD Protection of Power-managed High-voltage LDMOS Components," Electronics, vol. 12(13), pp. 2803-1–2803-13, Jun. 2023.
2. Jhong-Yi Lai, Shen-Li Chen*, Zhi-Wei Liu, Hung-Wei Chen, Hsun-Hsiang Chen, and Yi-Mu Lee, "Electrostatic-discharge Reliability Sensing of Ultrahigh-voltage N-channel Lateral-diffused MOSFETs Modulated by Different Operating Voltages," Sensors and Materials, vol. 34, no.5, pp.1835-1844, 2022.
3. Zhi-Wei Liu, Shen-Li Chen*, Jhong-Yi Lai, Hung-Wei Chen, Hsun-Hsiang Chen, and Yi-Mu Lee, "Electrostatic Discharge Sensing of Concentric Circles of Poly2 with Different Potentials and Discrete High-voltage P-well Modulation on Circular Ultrahigh-voltage N-channel Laterally Diffused MOSFET Devices," Sensors and Materials, vol. 34, no.5, pp.1823-1833, 2022.
4. Shen-Li Chen*, Po-Lin Lin, Hung-Wei Chen, and Yi-Mu Lee, "High Reliabilities Design of Stacked Ultra-high-voltage nLDMOSs in a 0.5-μm BCD Semiconductor Technology," Modern Concepts in Material Science, vol. 4(5), pp. 593-1–593-6, Nov. 2021.
5. Shi-Zhe Hong, Shen-Li Chen*, Hung-Wei Chen, and Yi-Mu Lee, "Drain Side Area-modulation Effect of Parasitic Schottky Diode on ESD Reliability for High Voltage P-channel Lateral-Diffused MOSFETs," IEEE Electron Device Letters, vol. 42(10), pp. 1512-1515, Oct. 2021.
6. Tien-Yu Lan, Shen-Li Chen*, Hung-Wei Chen, and Yi-Mu Lee, "Research on ESD Protection of Ultra-high Voltage nLDMOS Devices by Super-junction Engineering in the Drain-side Drift Region," IEEE Journal of the Electron Devices Society, vol.9, pp. 763-777, Aug. 2021.

7. Shi-Zhe Hong and Shen-Li Chen*, "ESD Design and Analysis by Drain Electrode-embedded Horizontal Schottky Elements for HV nLDMOSs," Electronics, vol. 10(1), pp. 178-1–178-15, Jan. 2021.
8. Po-Lin Lin, Shen-Li Chen* and Sheng-Kai Fan, "Enhance the ESD Ability of UHV 300-V Circular LDMOS Components by Embedded SCRs and the Robustness P-body Well," IEEE Journal of the Electron Devices Society, vol.9, pp. 108-113, Jan. 2021.
9. Po-Lin Lin, Shen-Li Chen* and Sheng-Kai Fan, "ESD-Performance Enhancement of Circular Ultra-High-Voltage 300-V N-Channel Lateral-Diffused MOSFETs by Source/Drain Embedded Schottky Diodes," IEEE Electron Device Letters, vol. 41(11), pp. 1673-1676, Nov. 2020.
10. Hung-Wei Chen, Shen-Li Chen*, Yu-Ting Huang, and Hsun-Hsiang Chen, "ESD improvements on power N-channel LDMOS devices by the Composite Structure of super junctions integrated with SCRs in the drain side," IEEE Journal of the Electron Devices Society, vol.8, pp. 864-872, Jul. 2020.
11. Shen-Li Chen* and S.P. Lee, "Optimized Design of the 100-V Silicon Based Power N-channel LDMOS Transistor," Modern Concepts in Material Science, vol. 3(2), pp. 559-1–559-6, Jul. 2020.
12. Shen-Li Chen*, Pei-Lin Wu and Yu-Jen Chen, "Robust ESD-Reliability Design of 300-V Power N-channel LDMOSs with the Elliptical Cylinder Super-junctions in the Drain Side," Electronics, vol. 9(4), pp. 730-1–730-14, Apr. 2020.
13. Sheng-Kai Fan, Shen-Li Chen*, Po-Lin Lin, and Hung-Wei Chen, "Layout Strengthening the ESD Performance for High-voltage N-channel Lateral Diffused MOSFETs," Electronics, vol. 9(4), pp. 718-1–718-20, Apr. 2020.
14. Po-Lin Lin, Shen-Li Chen* and Sheng-Kai Fan, "ESD-Immunity Impacts in 300 V nLDMOS by Comprehensive Drift-region Engineering," Electronics, vol. 8(12), pp. 1469-1-1469-14, 2019.
15. Shen-Li Chen*, Pei-Lin Wu, Yu-Lin Jhou, Po-Lin Lin and Sheng-Kai Fan, " ESD-Protection Design of UHV Circular N-channel LDMOSs by the Drift Region with Elliptical Cylinder Super-junctions," Advances in Technology Innovation, Dev. 2019 (accepted).
16. Shen-Li Chen*, Pei-Lin Wu and Po-Lin Lin, "ESD-Reliability Enhancement of Circular UHV 300-V Power nLDMOSs by the Drain-side Superjunction Structure," IEEE Electron Device Letters, vol. 40(4), pp. 597-600, Apr. 2019.
17. Shen-Li Chen*, Yi-Cih Wu, "Sensing and Reliability Improvement of Electrostatic-Discharge Transient by Discrete Engineering for High-Voltage 60-V N-Channel Lateral-Diffused MOSFETs with Embedded Silicon-Controlled Rectifiers," Sensors, vol. 18(10), pp. 3340-1-3340-10, Oct. 2018.
18. Shen-Li Chen*, Yu-Ting Huang, and Shawn Chang, "Design and Impact on ESD/LU Immunities by Drain-side Super-junction Structures in Low-(High-)Voltage MOSFETs for the Power Applications," IEICE Trans. on Electronics, vol. E101-C (3), pp. 141-150, Mar. 2018.

19. Shen-Li Chen*, Chun-Ju Lin, and Yu-Ting Huang, "Impacts of ESD Reliability by Different Layout Engineering in the 0.25-μm 60-V High-voltage LDMOS Devices," Physical Sciences Reviews, vol.3, issue 2, pp. 1-15, Feb. 2018.
20. Shen-Li Chen*, Yu-Ting Huang, and Yi-Cih Wu, "Design of High-ESD Reliability in HV Power pLDMOS Transistors by the Drain-side Isolated SCRs," IEICE Trans. on Electronics, vol. E100-C (5), pp. 446-452, May 2017.
21. Shen-Li Chen* and Min-Hua Lee, "Impacts of Leakage-Biasing Failure-mode Identification in the Transmission-Line Pulse Testing for Low-voltage/High-voltage MOSFET Components," IEEE Transactions on Industry Applications, vol. 53(3), pp.2888-2893, Mar. 2017.
22. Shen-Li Chen* and Shawn Chang, "Robust Reliability and Electrical Performances by the Bulk-Contact in 60-V p-channel LDMOS Power Components," International Journal of Green Energy, vol. 14(3), pp. 239-244, Mar. 2017.
23. Shen-Li Chen* and Dun-Ying Shu, "Measurement Forecast of Anomalous Threshold Voltages in BCD LV Submicron n-MOSFETs with Two Artificial Intelligence Methods", Measurement, vol. 100, pp. 93-98, Mar. 2017.
24. Shen-Li Chen*, Kuei-Jyun Chen, H.-W. Chen, "ESD Protection Design and Enhancement in the Power 60-V N-channel LDMOS by Embedded-SCR Anode Islands," Electronics Letters, vol. 52(19), pp. 1639-1640, Sep. 2016.
25. Shen-Li Chen* and Yu-Ting Huang, "Design and Layout Strategy in the 60-V Power pLDMOS with Drain-End Modulated Engineering of Reliability Considerations", IEEE Transactions on Power Electronics, vol. 31(7), pp.5113-5121, Jul. 2016.
26. Hung-Wei Chen, Yi- Mu Lee, and Shen-Li Chen, "The Taste Sensors with Conductivity Measurement," The Open Materials Science Journal, vol. 10, pp. 37-43, 2016.
27. Yeong-Lin Lai, Edward Y. Chang, Shen-Li Chen, K. B. Wang, Chun-Yi Zheng and Wen-Jung Chiang, "Characteristics of GaAs Power MESFETs with Double Silicon Ion Implantations for Wireless Communication Applications," The Open Materials Science Journal, vol. 10, pp. 29-36, 2016.
28. Shen-Li Chen*, Chin-Chai Chen, Yeong-Lin Lai, Wen-Jung Chiang and Hung-Wei Chen, "PL Intensity and Life-time Enhancements of the n-GaN Light-Emitting Diode During the Device Fabrication," The Open Materials Science Journal, vol. 10, pp. 20-28, 2016.
29. Shen-Li Chen*, "Editorial: Advanced Microelectronic and Nanoscale Semiconductor Materials & Applications," The Open Materials Science Journal, vol. 10, pp. 18-19, 2016.
30. Shen-Li Chen* and Min-Hua Lee, "ESD-Reliability Influences of an HV nLDMOS with Different Embedded SCR Structures in the Drain Side", International Journal of Electrical and Electronics Engineering Research, vol. 6 (2), pp. 37-44, Apr. 2016.
31. Shen-Li Chen* and Min-Hua Lee, "Reliability Analysis of P^+ Pickup on Anti-ESD Performance in Four CMOS Low-voltage Technology Nodes," IETE Journal of Research, vol. 62(6), pp. 752-761, Apr. 2016.

32. Shen-Li Chen* and Yu-Ting Huang, "Design of Reliability Improvement in HV p-channel LDMOS DUTs by a 0.25 μm 60-V BCD Process", International Journal of Electronics and Electrical Engineering, vol. 4 (3), pp. 210-214, Mar. 2016.
33. Shen-Li Chen*, Min-Hua Lee, and Chun-Ju Lin, "Protection Design of the SCR Cooperation on ESD Reliability Performance in Microelectronics of Low-voltage/High-voltage N-channel MOSFET Devices," Wulfenia (Journal), vol. 22 (12-pt.2), pp. 7-21, Dec. 2015.
34. Shen-Li Chen* and Yi-Sheng Lai, "Strengthen Anti-ESD Characteristics in an HV LDMOS with Super-Junction Structures," IEEE Transactions on Power Electronics, vol. 30 (5), pp. 2375-2382, May 2015.
35. Shen-Li Chen*, "The I-V Characteristic Prediction of BCD LV pMOSFET Devices Based on an ANFIS-Based Methodology", Advances in Fuzzy Systems, vol. 2015, pp. 824524-1 ~ 824524-8, Feb. 2015.
36. Shen-Li Chen*, Shawn Chang, Chun-Hsing Shih, Hsun-Hsiang Chen, "ESD-Reliability Analysis and Strategy of the GaN-based Light-Emitting Diodes", Key Engineering Materials, vols. 656-657, pp. 57-62, May 2015.
37. Shen-Li Chen*, Tsung-Shiung Lee, Yu-Ting Huang, "Impacts of MOS Device Characteristic Under Different Oxygen-Dose Participations in the Silicon Substrate", Key Engineering Materials, vols. 656-657, pp. 8-13, May 2015.
38. Shen-Li Chen*, Shawn Chang, Yu-Ting Huang, Shun-Bao Chang, "Reliability Enhancement in the 60 V Power pLDMOS by a Bulk-FOD Engineering," Advanced Materials Research, vols. 1079-1080, pp. 506-509, Jan. 2015.
39. Shen-Li Chen* and Hung-Wei Chen, "Pseudo-Failure Impacts on ESD Robustness in Integrated Circuits I/O Ports by the Parasitic Capacitance", The Open Electrical and Electronic Engineering Journal, vol. 8, pp. 143-251, Dec. 2014..
40. Shen-Li Chen*, "Enhanced Electrostatic Discharge Reliability in GaN-Based Light-Emitting Diodes by the Electrode Engineering", IEEE/OSA Journal of Display Technology, vol. 10, no.10, pp. 779-785, Oct. 2014.
41. Shen-Li Chen* and Chun-Ju Lin, "Layout Structure Dependence of 60-V nLDMOS Devices in the Anti-ESD Reliability Consideration", Journal of Electrical and Control Engineering, vol. 4(5), pp. 1-9, Oct. 2014.
42. Shen-Li Chen* and Shih-Hua Hsu, "Design of a High Performance Green-Mode PWM Controller IC with Smart Sensing Protection Circuits," Sensors and Transducers Journal, vol. 176, issue 8, pp. 210-218, Aug. 2014.
43. Shen-Li Chen* and Min-Hua Lee, "A Comprehensive Evaluation of Drain-side Layout Topologies on the Power nLDMOS ESD/LU Reliabilities," Research Journal of Applied Sciences, Engineering and Technology, vol. 8(4), pp. 496-502, Jul. 2014.
44. Shen-Li Chen* and Yi-Sheng Lai, "Anti-ESD Improvement of a Power nLDMOS with a Perpendicular Super-junction Construction in the Drain Side", Applied Mechanics and Materials, Vol. 595, pp. 195-200, Jun. 2014.

45. Shen-Li Chen*, Wen-Ming Lee and Chi-Ling Chu, "ESD Failure Analysis and Robustness Design in Vertical-Diffused MOS Transistors", Advanced Materials Research, Vols. 926-930, pp.456-461, Jun. 2014.
46. Shen-Li Chen*, Wen-Ming Lee, Chi-Ling Chu, "EMMI Failure-Distributed Analysis of ESD Zapping and Protection Designs in Power VDMOS ICs", International Journal of Energy Science, vol.4, issue 3, pp. 77-84, Jun. 2014.
47. Shen-Li Chen* and Dun-Ying Shu, "By Using Grey System and Fuzzy-Neural Network to Predict the Threshold Voltage of Complicated Sub-micron MOSFETs", WIT Transactions on Engineering Sciences, vol. 92, pp. 537-544, Jun. 2014.
48. Shen-Li Chen*, Wen-Ming Lee and Chi-Ling Chu, "ESD Hazard Analysis of VDMOS Power Components by Photoemission Spectroscopy", WIT Transactions on Information and Communication Technologies, vol. 56, pp. 721-728, May 2014.
49. Shen-Li Chen* and Min-Hua Lee, "Highly ESD Reliable HV Power nLDMOS Device with the Bulk FODs Design Technique", Energy Education Science and Technology, Part A: Energy Science and Research, vol. 32 (5), pp.3115-3124, May 2014.
50. Shen-Li Chen* and Min-Hua Lee, "ESD Reliability Improvement of an HV nLDMOS by the Bulk FODs Engineering", AASRI Procedia -Journal- Elsevier, USA, vol. 7, pp. 114-119, May 2014.
51. Shen-Li Chen* and Min-Hua Lee, "Impacts of the Drain-side nWell Adding on ESD Robustness in 0.25-μm LV/HV nMOSTs", AASRI Procedia -Journal- Elsevier, USA, vol. 7, pp. 51-56, May 2014.
52. Shen-Li Chen*, Min-Hua Lee, "Drain Side nWell Influences on the Reliability Immunity of 0.25-μm LV/HV GGnMOS Devices by TLP Testing and EDA Simulation", WIT Transactions on Modelling and Simulation, vol. 60, pp. 1181-1185, Apr. 2014.
53. Shen-Li Chen*, Der-Ann Fran, "Improvement on ESD Protection of Output Driver in DC Brushless Fan ICs by the FOD Protection Block", Advanced Materials Research, Vols. 850-851, pp.449-453, Mar. 2014.
54. Shen-Li Chen*, Min-Hua Lee, "Impact of Drain-side nWell Engineering on ESD Robustness in 0.35 μm LV MOSTs", Advanced Materials Research, Vols. 850-851, pp.7-11, Mar. 2014.
55. Shen-Li Chen* and Yang-Shiung Cheng, "Signal Sensing by the Architecture of Embedded I/O Pad Circuits", International Journal on Smart Sensing and Intelligent Systems, vol. 7, no. 1, pp.196-213, Mar. 2014.
56. Shen-Li Chen*, Min-Hua Lee, "A Novel ESD/LU Protection Structure with Drain FODs for High-voltage nLDMOS Applications", WIT Transactions on Information and Communication Technologies, vol. 49, pp. 533-540, Feb. 2014.
57. Shen-Li Chen*, Chun-Ju Lin, "Layout-type Dependence on ESD/LU Immunities for LVTnSCR Devices in LV Applications", WIT Transactions on Information and Communication Technologies, vol. 49, pp. 525-532, Feb. 2014.
58. Shen-Li Chen* and Der-Ann Fran, "Implementation of ESD Protection for Output Driver ICs with SCR Circuits Techniques", Applied Mechanics and Materials, vol. 464, pp.139-144, Feb. 2014.

59. Shen-Li Chen*, Yi-Sheng Lai, "Effects of Source Pick-up Adding and ESD Implanted Layer on ESD Reliability of LV GGnMOSTs", WIT Transactions on Engineering Sciences, vol. 87, pp. 175-182, Jan. 2014.
60. Shen-Li Chen*, Min-Hua Lee, "The Pick-up Strategy of Multi-finger GDpMOSTs on ESD Robustness in a 0.35 μm Process Technology", WIT Transactions on Engineering Sciences, vol. 87, pp. 165-173, Jan. 2014.
61. Shen-Li Chen*, Min-Hua Lee, "Impact of FODs Adding on the ESD/LU Reliabilities in 0.35 μm 3.3 V LV nMOSTs", WIT Transactions on Engineering Sciences, vol. 87, pp. 155-163, Jan. 2014.

B. Book Chapter Series: (2014~2023)

1. Shen-Li Chen*, "The I-V Characteristic Prediction of BCD LV pMOSFET Devices based on an ANFIS-Based Methodology," Prime Archives in Electronics, (ISBN: 978-93-90014-22-4), pp.1-20, Hyderabad, India, Jan. 2021.
2. Shen-Li Chen*, Pei-Lin Wu and Yu-Jen Chen, "Robust ESD-Reliability Design of 300-V Power N-channel LDMOSs with the Elliptical Cylinder Super-junctions in the Drain Side," Industrial Applications of Power Electronics (ISBN: 978-3-03943-483-1), pp. 265-278, MDPI Publisher(Editor: Eduardo M. G. Rodrigues), Basel, Switzerland, Dec. 2020.
3. Po-Lin Lin, Shen-Li Chen* and Sheng-Kai Fan, "ESD-Immunity Impacts in 300 V nLDMOS by Comprehensive Drift-region Engineering," Intelligent Electronic Devices (ISBN: 978-3-03928-973-8), pp. 91-104, MDPI Publisher(Editor: Teen-Hang Meen), Basel, Switzerland, May 2020.
4. Shen-Li Chen*, Yi-Cih Wu, "Sensing and Reliability Improvement of Electrostatic-Discharge Transient by Discrete Engineering for High-Voltage 60-V N-Channel Lateral-Diffused MOSFETs with Embedded Silicon-Controlled Rectifiers," Top 5 Contributions on Sensor and Biosensor Technology, 2nd Edition (ISBN: 978-93-88170-19-2), pp. 2-22, AVID SCIENCE Publisher(Editor: Priyanka), Berlin, Germany, Dec. 2018.
5. Shen-Li Chen*, Chun-Ju Lin, and Yu-Ting Huang, "Impacts of ESD Reliability by Different Layout Engineering in the 0.25-μm 60-V High-voltage LDMOS Devices," Nano Devices and Sensors (ISBN 978-1-5015-1050-2), pp. 177-197, De Gruyter Publisher, Berlin, Germany, Mar. 2016.
6. Shen-Li Chen*, Shawn Chang, Yu-Ting Huang, Shun-Bao Chang, "Anti-ESD Improvement by the Bulk-FOX Structure in HV nLDMOS Devices," Lecture Notes in Electrical Engineering (ISBN: 978-3-319-17313-9), vol. 345, Chap. 73, pp.571-577, New York, USA, Springer publisher, Jan. 2016.
7. Shen-Li Chen*, Yu-Ting Huang, Shawn Chang, Shun-Bao Chang, "N+ Extended-Distribution Influences on Anti-ESD Ability in the 60-V pLDMOS-SCR (NPN arranged-type)," Lecture Notes in Electrical Engineering (ISBN: 978-3-319-17313-9), vol. 345, Chap. 74, pp.579-585, New York, USA, Springer publisher, Jan. 2016.

8. Shen-Li Chen*, Min-Hua Lee, Chun-Ju Lin, Yi-Sheng Lai, Shawn Chang, and Yu-Ting Huang, "ESD Performance Influence of a 60-V Lateral-diffused-MOST by the FOD Based (& Dotted-OD) Drain", Lecture Notes in Electrical Engineering-Intelligent Technologies and Engineering Systems (ISBN: 978-3-319-04572-6), vol. 293, Chap. 108, pp.883-890, New York, USA, Springer publisher, 2014.
9. Shen-Li Chen*, Min-Hua Lee, Yi-Sheng Lai, Chun-Ju Lin, Yu-Ting Huang, and Shawn Chang, "Effect of Drain FODs on ESD/LU Immunities in the 60V High-voltage nLDMOS", Lecture Notes in Electrical Engineering- Intelligent Technologies and Engineering Systems (ISBN: 978-3-319-04572-6), vol. 293, Chap. 107, pp.875-882, New York, USA, Springer publisher, 2014.

C. Referred Conference Papers: (2014~2023)

1. 楊修源, 陳勝利*, 林廷恩, "高壓 nLDMOS 汲極端水平嵌入離散 P^+ SCR 之抗 ESD/栓鎖效應可靠度研究," 中國機械工程學會第四十屆全國學術研討會, Changhua, Taiwan, Dec. 2023, pp.927-929.
2. 林廷恩, 陳勝利*, 楊修源, "高壓 nLDMOS 汲極端嵌入 STI 面積調變對可靠度增強之研究," 中國機械工程學會第四十屆全國學術研討會, Changhua, Taiwan, Dec. 2023, pp.930-932.
3. 陳勛祥, 林家丞, 陳勝利, "10 位元 10MHz 取樣頻率之 CMOS 導管式類比數位轉換器設計," 中國機械工程學會第四十屆全國學術研討會, Changhua, Taiwan, Dec.. 2023, pp.933-935.
4. 林廷恩, 陳勝利*, 劉誌瑋, 楊修源, "高壓 nLDMOS 汲極端寄生 Schottky/SCR 面積調變之抗 ESD 能力探討," T-ESD & Reliability Conference, Hsinchu, Taiwan, Nov. 2023, pp.C3-1- C3-4.
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D. Patents 專利 : (2014~2023)

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2. 陳昱臻, 林吉聰, 陳勝利, "簡化型蕭特基能障穿隧塊材式場效電晶體", 中華民國新型專利, 證書# TW M598528, pp. 12396-12401, 2020.07.11～2030.04.14.
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6. 陳勝利, "具有可控硅结构之高压半导体器件", 中华人民共和国实用新型专利, 證書# CN 205303464 (ZL2015-2-1085705.4), pp. 1～11, (2015.12.23～2024.12.22).
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10. 陳勝利, "高壓半導體元件", 中華民國新型專利, 證書# TW M488745, pp. 14915-14920, Oct. 2014, (2014.10.21 ~ 2024.07.14).
11. 陳勝利, "發光二極體", 中華民國新型專利, 證書# TW M487526, pp. 16151-16157, Oct. 2014 (2014.10.01 ~ 2024.05.25).
12. 陳勝利, "具有高靜電放電防護能力的半導體結構", 中華民國新型專利, 證書# TW M482841, pp. 14786-14788, Jul. 2014 (2014.07.21 ~ 2024.01.07).

E. Research Projects (研究計劃)：(2011~2023)

年度	補助類別	計畫名稱	擔任工作	執行期間
112	國科會專題研究計畫 (一般型研究計畫)	BCD 高壓製程之電源管理 IC 30-90V 輸出埠八邊型 LDMOS 組件強化抗 ESD/ Latch-up 可靠度能力提升研究 (NSTC 112-2221-E-239-004)	計劃主持人	112/08/01 ~ 113/07/31
111	科技部專題研究計畫 (一般型研究計畫)	電極內建蕭特基/SCR 架構可靠度設計之電源管理應用圓形超高壓功率 LDMOS 組件研究 (MOST 111-2221-E-239 -014)	計劃主持人	111/08/01 ~ 112/07/31
110	科技部專題研究計畫 (一般型研究計畫)	電源管理系統輸出級 200V~300V 橢圓超高壓功率 LDMOS 組件之抗 ESD 工程設計研究 (MOST 110-2221-E-239-013)	計劃主持人	110/08/01 ~ 111/07/31
109	科技部專題研究計畫 (一般型研究計畫)	高 ESD 防護能力設計之電源轉換應用 100V~300V 超高壓 nLDMOS 組件研究 (MOST 109-2221-E-239-015)	計劃主持人	109/08/01 ~ 110/07/31
108	科技部專題研究計畫 (一般型研究計畫)	電源管理應用上圓形超高壓功率 LDMOS 組件高可靠度設計研究 (MOST 108-2221-E-239-012)	計劃主持人	108/08/01 ~ 109/07/31
107/11~109/10	康舒科技股份有限公司	PWM 控制晶片設計所需的高壓靜電放電保護元件研究 (A107-1055)	計劃主持人	107/11~109/10
106	力晶科技公司	開發 ESD 防護元件在 55nm/40nm 高壓平台	計劃主持人	106/1~ 108/12
106	科技部專題研究計畫 (一般型研究計畫)	電力轉換超高壓 LDMOS 高抗靜電可靠度防護工程研究 (MOST 106-2221-E-239-018)	計劃主持人	106/08/01 ~ 107/07/31
105	科技部專題研究計畫 (一	電源管理功率積體電路輸出驅動埠電性與高可靠度能力提升研究	計劃主持人	105/08/01 ~ 106/07/31

	般型研究計畫)	(MOST 105-2221-E-239-017)		
105	鉅晶科技公司	0.18um 6V_40V(6V_18V_60V) 功率製程 ESD 全晶片防護(元件)設計開發 (A105-1024)	計劃主持人	105/04~107/01
104	科技部專題研究計畫 (一般型研究計畫)	綠能組件電源埠防護佈局工程與抗ESD 能力模型化研究 (MOST 104-2221-E-239-013)	計劃主持人	104/08/01 ~ 105/07/31
103	科技部專題研究計畫 (一般型研究計畫)	高壓製程電源管理組件之結構調變可靠度影響研究 (MOST 103-2221-E-239 -014)	計劃主持人	103/08/01 ~ 104/07/31
102	國科會專題研究計畫 (一般型研究計畫)	照明高壓驅動組件高可靠度佈局工程研究 (NSC 102-2221-E-239 -015)	計劃主持人	102/08/01 ~ 101/07/31
100	國科會專題研究計畫 (一般型研究計畫)	高可靠性低驟回之車用高壓 nLDMOS 元件研究 (NSC 100-2221-E-239 -003)	計劃主持人	100/08/01 ~ 101/07/31