劉仁傑 (Prof. Jen-Chieh Liu)

Phone: +886-37382480 (O)

Dept. of Electrical Engineering, National United U.

2 Lien-Da Rd., MiaoLi City 36063, Taiwan

EMail: jcliu@nuu.edu.tw

I. Main Education (學歷)

- 「國立中央大學-電機工程學系」博士 (95~101)
- 「私立輔仁大學-電子工程學系」碩士 (93~95)
- 「私立輔仁大學-電子工程學系」學士 (89~93)

II. Research Fields (Expertise 研究專長)

- 數位/類比積體電路設計
- 時脈電路與低功率晶片設計

III. Personal Experiences (履經歷):

- 「國立聯合大學-電機工程學系」副教授 (107~迄今)
- 「國立聯合大學-電機工程學系」助理教授 (103~107)
- 「工業技術研究院-資訊與通訊研究所」工程師 (99~103)

IV. Personal Honors (個人榮譽事項)：

1.「106 年度國立聯合大學電機資訊學院」榮獲國際競賽傑出獎 第一名。

2.「106 年度國立聯合大學電機資訊學院」榮獲研究躍進獎 第二名。

3.「103 年度智慧電子跨領域應用專題系列課程計畫」榮獲計畫類優等。

4.「102 年度電腦與通訊期刊最佳論文獎」榮獲佳作論文獎。

5.「工研院 102 年傑出研究獎」榮獲工研精英金牌獎。

6.「工研院第十屆品質典範案例」榮獲產業科技研發類優勝佳作獎。

7.「國家晶片系統設計中心 2011 晶片製作」榮獲數位組優良設計獎。

8.「國家晶片系統設計中心 2011 晶片製作」榮獲類比組佳作設計獎。

9.「中央大學 98 學年度第二學期」榮獲優秀學生獎學金。

10.「The 18th VLSI Design/CAD Symposium 會議」榮獲最佳論文獎。

11.「國家晶片系統設計中心 2007 晶片製作」榮獲數位組優良設計獎。

12.「95 學年度中華民國斐陶斐榮譽學會」榮獲榮譽會員。

13.「輔仁大學電子工程學系之 2006 論文研究成果發表」，榮獲最佳壁報製作獎。

14.「輔仁大學 93 學年度第二學期」榮獲成績優異獎學金。

15.「教育部 94 學年度 SIP 設計競賽」榮獲優等獎。

16.「教育部 94 學年度大學院校積體電路設計競賽」，榮獲研究所 Full-custom 組佳作獎。

17.「教育部 92 學年度大學院校積體電路設計競賽」，榮獲大學部 Full-custom 組優等獎。

VI. Publication Papers & Projects (近年發表之論文與研究計劃)

A. Journal Papers:

1. **Jen-Chieh Liu*** and Chuan Yang, “A digital delay locked loop with a monotonic delay line,” *IEE Electronics Letters*, vol. 59, no.11, pp. 1-3, Jun. 2023. (SCI)
2. Hong-Yi Huang, **Jen-Chieh Liu***, Fu-Chien Tsai, Kun-Hua Lee and Kun-Yuan Chen, “A 12-phase and 5-GHz PLL with a subfeedback loop technique,” *Circuits, Systems, and Signal Processing*, vol. 42, no.4, pp.1873-1892, April. 2023. (SCI)
3. **Jen-Chieh Liu*** and Yan-Xun Chen, “DPLL-based VRO of time-to-digital converter,” *IEEE Solid-State Circuits Letters*, vol. 6, pp. 45-48, Feb. 2023. (ESCI)
4. Yu-Lung Lo, Fang-Yu Fan, Hsi-Hua Wang, Yu-Hsin Li, Zi-Yi Chen, and **Jen-Chieh Liu**, “A fast-lock low-power all-digital DLL-based clock generator with fractional multiple technique,” *Microsystem Technologies*, vol. 27, no.4, pp.1335-1346, April. 2021. (SCI)

5. Yu-Lung Lo, Yu-Hsin Li, Fang-Yu Fan, Chun-Yen Yu, and **Jen-Chieh Liu***, “A low-jitter all-digital PLL with high-linearity DCO,” *Microsystem Technologies*, vol. 27, no.4, pp.1347-1357, April. 2021. (SCI)

6. **Jen-Chieh Liu*** and Yu-Ping Li, “A low supply voltage all-digital phase-locked loop with a bootstrapped and forward interpolation digitally controlled oscillator,” *IEEE Access*, vol. 9, no.3, pp. 39717-39726, Mar. 2021. (SCI)

7. Yo-Hao Tu, **Jen-Chieh Liu***, Kuo-Hsing Cheng and Chi-Yang Chang, “A low supply voltage and multiphase all-digital crystal-less clock generator,” *IET Circuits, Devices and Syst.*, vol. 12, no. 6, pp. 720-725, Dec. 2018. (SCI)

8. Yo-Hao Tu, Kuo-Hsing Cheng, Man-Ju Lee and **Jen-Chieh Liu***, “A power-saving adaptive equalizer with a digital-controlled self-slope detection,” *IEEE Trans. on Circuits and Syst. I*, vol. 65, no.7, pp. 2097-2108, July 2018. (SCI)

9. **Jen-Chieh Liu***, Chao-Jen Huang, and Pei-Ying Lee, “A high accuracy programmable pulse generator with a 10 ps timing resolution,” *IEEE Trans. on Very Large Scale Integr. (VLSI) Syst*., vol. 26, no.4, pp. 621-629, Apr. 2018. (SCI)

10. Yo-Hao Tu, **Jen-Chieh Liu***, Kuo-Hsing Cheng, and Chih-Hsun Hsu, “A 0.5-V all-digital clock-deskew buffer with I/Q phase outputs,” *Analog Integrated Circuits and Signal Processing*, vol. 93, no.10, pp.157-167, Oct. 2017. (SCI)

11. Ting-Chou Lu, Ming-Dou Ker, Hsiao-Wen Zan, **Jen-Chieh Liu***, and Yu Lee, “A 8 phases 192 MHz crystal-less clock generator with PVT calibration,” *IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences*, E100-A (1), pp. 275-282, Jan. 2017. (SCI)

12. **Jen-Chieh Liu***, and Pei-Ying Lee, “A low power pulse generator for test platform applications,” *IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences*, E99-A (7), pp.1415-1416, Jul. 2016. (SCI)

13. Yo-Hao Tu, **Jen-Chieh Liu***, and Kuo-Hsing Cheng, “Proportional static-phase-error reduction for frequency-multiplier-based delay-locked-loop architecture,” *IEICE Trans. on Electronics*, E99-C (6), pp.655-658, Jan. 2016. (SCI)

14. Yo-Hao Tu, **Jen-Chieh Liu***, Kuo-Hsing Cheng, Hong-Yi Huang, Chang-Chien Hu, “A 0.6-V 1.6-GHz 8-phase all digital PLL using multi-phase based TDC,” *IEICE Electronics Express*, vol. 13, no.2, pp.1-12, Jan. 2016. (SCI)

15. Kuo-Hsing Cheng, Cheng-Liang Hung*, Cihun-Siyong Alex Gong, **Jen-Chieh Liu**, Bo-Qian Jiang, and Shi-Yang Sun, “A 0.9-8 GHz VCO with a differential active inductor for multistandard wireline SerDes,” *IEEE Trans. on Circuits and Syst. II*, vol. 61, no.8, pp.559-563, Ang. 2014. (SCI)

16. Kuo-Hsing Cheng, **Jen-Chieh Liu***, Hong-Yi Huang, and Yu-Tso Chen, “A wide supply voltage range and low-power all-digital clock generator,” *Analog Integrated Circuits and Signal Processing*, vol. 74, no.3, pp.517-526, Mar. 2013. (SCI)

17. Kuo-Hsing Cheng, **Jen-Chieh Liu***, and Hong-Yi Huang, “A 0.6-V 800-MHz all-digital phase-locked loop with a digital supply regulator,” *IEEE Trans. on Circuits and Syst. II*, vol.59, no.12, pp.888-892, Dec. 2012. (SCI)

18. Hong-Yi Huang* and **Jen-Chieh Liu**, “All-digital PLL using bulk-controlled varactor and pulse-based digitally controlled oscillator,” *Analog Integrated Circuits and Signal Processing*, vol. 68, no.3, pp.245-255, Sep. 2011. (SCI)

19. Kuo-Hsing Cheng, **Jen-Chieh Liu***, Hong-Yi Huang, Yu-Liang Li and Yong-Jhen Jhu, “A 6 GHz built-in jitter measurement circuit using multi-phase sampler,” *IEEE Trans. on Circuits and Syst. II*, vol.58, no.8, pp.492-496, Aug. 2011. (SCI)

20. Kuo-Hsing Cheng, **Jen-Chieh Liu***, Chih-Yu Chang, Shu-Yu Jiang, and Kai-Wei Hong, “Built-in jitter measurement circuit with calibration techniques for a 3-GHz clock generator,” *IEEE Trans. on Very Large Scale Integr. (VLSI) Syst.*, vol.19, no.8, pp.1325-1335, Aug. 2011. (SCI)

21. Kuo-Hsing Cheng, Kai-Wei Hong*, Chi-Hsiang Chen, and **Jen-Chieh Liu**, “A high precision fast locking arbitrary duty cycle clock synchronization circuit,” *IEEE Trans. on Very Large Scale Integr. (VLSI) Syst.*, vol.19, no.7, pp.1218-1228, July 2011. (SCI)

B. Book Series Papers:

C. Conference Papers:

1. Bo-Jun Huang, Wen-Yuan Tsai and **Jen-Chieh Liu**, “A 0.5-V 3-GHz digital PLL with a subfeedback loop technique,” *13th International Conference on Information and Electronics Engineering*, accepted to 2024.

2. Rui-Cheng Ai , Zhe-yuan Jin and **Jen-Chieh Liu**, “Design of PLL with a power-down scheme,” *13th International Conference on Information and Electronics Engineering*, accepted to 2024.

3. Wen-dong Ke and **Jen-Chieh Liu**, “A crystal-less clock generator using a relaxation oscillator,” *13th International Conference on Information and Electronics Engineering*, accepted to 2024.

4. **Jen-Chieh Liu**, Yu-Hsiang Tseng, and Wen-Yuan Tsai, “A boost DC-DC converter using PFM control scheme,” *International Conference on Power and Energy Systems Engineering*, pp. 1, Sep. 2019.

5. Jian-Sheng Li and **Jen-Chieh Liu**, “A wide input range digital time-to-digital converter wireless network technology,” *International Conference on Information and Electronics Engineering*, pp. 37, Feb. 2019.

6. Yu-Ping Li, Yu-Han Liu, and **Jen-Chieh Liu**, “An integer-N phase-locked loop with automatic VCO band selection,” *International Conference on Information and Electronics Engineering*, pp. 33, Feb. 2019.

7. Yo-Hao Tu, Kuo-Hsing Cheng, Wei-Ren Wang, **Jen-Chieh Liu**, and Hong-Yi Huang, “A chaotically injected timing technique for ring-based oscillators,” *IEEE Symposium on Design and Diagnostics of Electronic Circuits and System*, pp. 1-4, Jun. 2016.

8. Hong-Yi Huang, **Jen-Chieh Liu**, Pei-Ying Lee, Kun-Yuan Chen, Jin-Sheng Chen, Kuo-Hsing Cheng, Tzuen-Hsi Huang, Ching-Hsing Luo, and Jin-Chern Chiou, “PVT Insensitive high-resolution time to digital converter for intraocular pressure sensing” *IEEE Symposium on Design and Diagnostics of Electronic Circuits and System*, pp. 125-128, Apr. 2015.

9. **Jen-Chieh Liu**, Huan-Ke Chiu, Jia-Hung Peng, Yuan-Hua Chu, and Hong-Yi Huang, “A radio-controlled receiver for clocks/watches and alarm applications,” *IEEE International Symposium on Circuits and Systems,* pp. 2672-2675, Jun. 2014.

10. Hong-Yi Huang, **Jen-Chieh Liu**, Shi-Jia Sun, Cheng-Hao Fu, and Kuo-Hsing Cheng, “A 64-MHz ~ 640-MHz 64-phase clock generator” *IEEE Symposium on Design and Diagnostics of Electronic Circuits and System*, pp. 51-54, Apr. 2014.

11. **Jen-Chieh Liu**, Wei-Chun Lee, Hong-Yi Huang, Kuo-Hsing Cheng, Chao-Jen Huang, Yu-Wei Liang, Jia-Hung Peng, and Yuan-Hua Chu, “A 0.3-V all digital crystal-less clock generator for energy harvester applications” *IEEE Asian Solid-state Circuits Conference*, pp.117-120, Dec. 2012.

12. Chih-Ping Cheng, **Jen-Chieh Liu**, and Kuo-Hsing Cheng, “Auto-calibration techniques in built-in jitter measurement circuit” *IEEE Symposium on Design and Diagnostics of Electronic Circuits and System*, pp.248-249, Apr. 2012.

13. Tzu-Chi Huang, Hong-Yi Huang, **Jen-Chieh Liu**, Kuo-Hsing Cheng, and Ching-Hsing Luo, “All digital phase-locked loop using active inductor oscillator and novel locking algorithm,” *IEEE International Symposium on Circuits and Systems,* pp. 486-489, May 2011.

14. Kuo-Hsing Cheng, Chih-Yu Chang, **Jen-Chieh Liu**, and Chih-Ping Cheng, “Measurement error analysis and calibration techniques for built-in jitter measurement circuit” *IEEE International Symposium on VLSI Design Automation & Test*, pp.1-4, Apr. 2011.

15. Kai-Wei Hong, Kuo-Hsing Cheng, Chi-Hsiang Chen, **Jen-Chieh Liu**, and Chien-Cheng Chen, “Loading effect insensitive an d high precision clock synchronization circuit” *IEEE European Solid-State Circuits Conference*, pp.514-517, Sep. 2010.

16. Kuo-Hsing Cheng, Chang-Chien Hu, **Jen-Chieh Liu**, and Hong-Yi Huang, “A time-to-digital converter using multi-phase-sampling and time amplifier for all digital phase-locked loop” *IEEE Symposium on Design and Diagnostics of Electronic Circuits and System*, pp.285-288, Apr. 2010.

17. **Jen-Chieh Liu**, Hong-Yi Huang, Wei-Bin Yang and Kuo-Hsing Cheng, “ 0.5 V 160-MHz 260 uW all digital phase-locked loop ” *IEEE Symposium on Design and Diagnostics of Electronic Circuits and System*, pp.186-193, Apr. 2009.

18. Hong-Yi Huang, **Jen-Chieh Liu**, and Kuo-Hsing Cheng, “All digital PLL using pulse-based DCO” *IEEE International Conference on Electronic*s, *Circuits and Systems*, pp.1268-1271 Dec. 2007.

19. Hong-Yi Huang, Bo-Ruei Wang and **Jen-Chieh Liu**, “High-gain and high-bandwidth rail-to-rail operational amplifier with slew rate boost circuit,” *IEEE International Symposium on Circuits and Systems,* pp. 21-24, May 2006.

D. Patents 專利：

1. 劉仁傑，張啟揚，涂祐豪，鄭國興，”非石英時脈產生器及其運作方法”中華民國，發明第 I 520495 B 號，2016。
2. **Jen-Chieh Liu**, Chi-Yang Chang, Yo-Hao Tu, and Kuo-Hsing Cheng, “All digital crystal-less clock generator using temperature compensated techniques,” *US Patent, , US 9,024,693,* 2015.
3. Hong-Yi Huang, **Jen-Chieh Liu**, and Yuan-Hua Chu, “High-resolution varactors, single-edge triggered digitally controlled oscillators, and all-digital phase-locked loops using the same,” *US Patent,* US 8,125,286, 2012.
4. 黃弘一，劉仁傑，朱元華，”數位控制振盪器和全數位鎖相迴路”中華人民共和國，專利號 ZL 2007 1 0088558.X，2011。
5. 黃弘一，劉仁傑，朱元華，”數位控製變容器、數位控制振盪器和全數位鎖相迴路”中華民國，發明第 I 348276 號，2011。
6. Hong-Yi Huang, **Jen-Chieh Liu**, and Yuan-Hua Chu, “High-resolution varactors, single-edge triggered digitally controlled oscillators, and all-digital phase-locked loops using the same,” *US Patent,* US 7,859,343, 2010.

E. Award 獎項：

1. 指導 陳淇樺與林科男 同學　獲得「教育部 112 學年度大學院校積體電路設計競賽」，榮獲研究所 Full-custom 組，佳作。
2. 指導 劉軒誠 同學　獲得「112 年度科技部大專學生研究計畫」補助。
3. 指導 陳彥勳與陳淇樺 同學　獲得「教育部 111 學年度大學院校積體電路設計競賽」，榮獲研究所 Full-custom 組，完成獎。
4. 指導 李玉萍 同學　獲得「國研院台灣半導體研究中心 2020 晶片製作」榮獲類比/混合訊號類特優設計獎。
5. 指導 陳彥勳 同學　獲得「國家中山科學研究院 108 年度延攬大學院校優秀學生獎助金」補助。
6. 指導 吳姿靜 同學　獲得「108 年度科技部大專學生研究計畫」補助。
7. 指導 李建陞與蔡和成 同學　獲得「教育部 107 學年度大學院校積體電路設計競賽」，榮獲研究所 Full-custom 組完成獎。

8. 指導 劉玉涵 同學　獲得「教育部 107 學年度大學院校積體電路設計競賽」，榮獲研究所 Full-custom 組完成獎。

9. 指導 李玉萍與劉玉涵 同學　獲得「經濟部技術處“2016 搶鮮大賽”大專院校組-創意發想類」優勝。

10. 指導 李玉萍 同學 獲得「2016 IEEE International Conference on Applied System Innovation」 First Prize Paper Award。

11. 指導 曾御翔 同學　獲得「105 年度科技部大專學生研究計畫」補助。

12. 指導 李玉萍 同學　獲得「104 年度科技部大專學生研究計畫」補助。

F: Research Projects:

112-113 年度，科技部，「多通道測試訊號產生器之設計」（1239k nt）

112-113 年度，致茂電子，「半導體測試晶片研究計畫」（1320k nt）

111 年度，致茂電子，「半導體測試晶片研究計畫」（660k nt）

111 年度，科技部，「四通道之訊號產生器與其可程式化之延遲電路」（631k nt）

110 年度，科技部，「無需參考訊號之低電壓時脈產生器」（688k nt）

108 年度，科技部，「寬操作電壓與多相位之數位式鎖相迴路」（863k nt）

107 年度，工研院，「時序合成技術」(360k nt)

107 年度，工研院，「人材培育計畫-碩士生工程人才」(360k nt)

107 年度，科技部，「高時間解析度之信號產生器」（690k nt）

106 年度，工研院，「ULP/High Accuracy PFIC 技術」(250k nt)

106 年度，科技部，「高可靠度之車用時脈電路」（630k nt）

105 年度，工研院，「高可靠震盪器電路」(650k nt)

104 年度，科技部，「寬操作電壓之非石英式數位時脈產生器」（633k nt）

104 年度，教育部(協同主持人)，「智慧電子跨領域應用專題系列課程計畫」（2656k nt）

104 年度，工研院，「CLCG 與 ADPLL 電路技術開發計畫」（650k nt）

103 年度，工研院，「多相位無震盪器時脈產生器電路設計」（200k nt）